IN THE SPECIFICATION:

Please amend paragraph number **[0002]** as follows:

**[0002]** State of the Art: Capacitors are used in a wide variety of semiconductor circuits, such as in dynamic random access memory ("DRAM") ~~memory~~ circuits. While the invention herein is discussed in relation to DRAM ~~memory~~ circuits, the applicability of the invention is not limited to DRAM ~~memory~~ circuits and may be used in any other type of memory circuits, such as static random access memory ("SRAM") ~~memory~~ circuits or any other circuits in which capacitors are used.

Please amend paragraph number **[0003]** as follows:

**[0003]** DRAM ~~memory~~ circuits are manufactured by replicating millions of identical circuit elements, known as DRAM cells, on a single semiconductor wafer. A DRAM cell, usually consisting of a single metal-oxide semiconductor field effect transistor ("MOSFET") and a single capacitor, is an addressable location that can store one bit (binary digit) of data. The DRAM cell stores a bit of data on the capacitor as an electrical charge. Manufacturing of the DRAM cell typically includes fabricating a transistor, a capacitor, and three contacts: one contact each to a bit line, a word line, and a reference voltage. DRAM manufacturing is a highly competitive business and there is continuous pressure to decrease the size of individual cells and increase memory cell density to allow more memory to be squeezed onto a single memory chip. However, it is also necessary to maintain a sufficiently high storage capacitance to maintain a charge at the refresh rates currently in use even as cell size continues to shrink. This requirement has led DRAM manufacturers to turn to three-dimensional capacitor designs, including trench and stacked capacitors. Stacked capacitors are capacitors that are stacked, or placed, over an access transistor in a semiconductor device. In contrast, trench capacitors are formed in the wafer substrate beneath the transistor. For reasons including ease of fabrication and increased capacitance, most manufacturers of DRAMs larger than 4 Megabits use stacked capacitors.

Please amend paragraph number **[0004]** as follows:

**[0004]** A widely used type of stacked capacitor is known as a container capacitor. Container capacitors are typically in the shape of an upstanding tube or cylinder having an oval or circular cross section. FIG. 1 illustrates a top view of a portion of a DRAM ~~memory~~ circuit from which the upper layers have been removed to reveal container capacitors 12 arranged around a bit line contact 14. Six container capacitors 12 are shown in FIG. 1, each of which is labeled with separate reference designations A to F. In FIG. 1, the bit line contact 14 is shared by DRAM cells corresponding to container capacitors A and B. The wall of each cylinder consists of two layers or plates of conductive material, such as doped polycrystalline silicon (referred to herein as "polysilicon" or "poly") separated by a dielectric layer. One of the plates is a bottom electrode while the second of the plates is a top electrode. The bottom end of the cylinder is closed, with the bottom electrode of the cylinder in contact with either a drain of the access transistor or a plug, which itself is in contact with the drain. The other end of the cylinder is open. Later in the fabrication process, the open end of the cylinder is filled with an insulative material. The sidewall and closed end of the cylinder form a container, which leads to the name "container capacitor." Although the invention will be further discussed in connection with stacked container capacitors, it is understood that the invention is not limited thereto. For example, use of the invention in trench capacitors is also possible.

Please amend paragraph number **[0005]** as follows:

**[0005]** In addition to being conductive, the bottom and top electrodes in the DRAM cell capacitor protect the dielectric layer from interaction with interlayer dielectrics (e.g., borophosphosilicate glass ("BPSG")) and from the harsh thermal processing encountered in subsequent processing. For instance, tantalum pentoxide ("$Ta_2O_5$") is commonly used in the dielectric layer for high density DRAMs, such as 64 Mbit and 256 Mbit DRAMs, because chemical vapor deposition ("CVD") of $Ta_2O_5$ provides a high dielectric constant (about 20-25) and good step coverage. However, when rapid thermally processed nitride ("RTN") is formed over a layer of hemispherical grain polysilicon ("HSG") to serve as an HSG barrier layer to prevent oxidation of

HSG during subsequent $Ta_2O_5$ deposition, there is a capacitance loss due to the RTN layer on the capacitor electrode. The effective dielectric constant for an RTN/$Ta_2O_5$ stack capacitor is about ~~10-12.~~ 10-12.

Please amend paragraph number **[0008]** as follows:

**[0008]** The present invention, in one embodiment, relates to a method of forming a ~~double-sided~~ double-sided capacitor. The method comprises forming at least one opening in an insulating layer on a semiconductor wafer. A sacrificial liner is formed along sidewalls of the at least one opening. The sacrificial liner is formed from a material, for example, such as titanium nitride, polysilicon or hemispherical grain polysilicon. A first conductive layer having a first surface and a second surface is then formed over the sacrificial liner, with the first surface of the first conductive layer contacting the sacrificial liner. The sacrificial liner is then selectively removed using, for example, a solution of hydrogen peroxide and sulfuric acid or a solution of tetramethylammonium hydroxide to expose the first surface of the first conductive layer. The sacrificial liner is selectively removed without damaging exposed components on the semiconductor wafer, such as the first conductive layer. Removing the sacrificial liner forms an open space adjacent to the first surface of the first conductive layer. A dielectric layer is formed in the open space, over the first and second surfaces of the first conductive layer. A second conductive layer is formed over the dielectric layer, producing the double-sided capacitor.

Please amend paragraph number **[0011]** as follows:

**[0011]** In another embodiment, the present invention relates to a method of forming a contact. The method comprises forming a first opening in a first insulating layer on a semiconductor wafer. A sacrificial liner is formed along sidewalls of the first opening from a material, such as, for example, titanium nitride, polysilicon or hemispherical grain polysilicon. A sacrificial plug is formed adjacent to the sacrificial liner. The sacrificial plug is formed from a material having a different etch selectivity than a material used in the sacrificial liner. A second insulating layer is formed over the first insulating layer and a second opening is formed in the

second insulating layer, the second opening in substantial alignment with the first opening. The sacrificial plug or both the sacrificial plug and the sacrificial liner are removed from the first opening without damaging exposed components on the semiconductor wafer. A conductive material is deposited in the first and second openings, forming the contact.

Please amend paragraph number **[0021]** as follows:

**[0021]** The material used in the sacrificial structure may be selected so that the sacrificial structure is removable from the opening without removing or damaging other components or portions of the semiconductor wafer. In other words, etching conditions used to remove the sacrificial structure may be chosen based on the material of the sacrificial structure and the materials of the other components on the semiconductor wafer. For instance, the sacrificial structure may be selectively removed without removing or damaging a bottom electrode of the double-sided capacitor. For sake of example only, the sacrificial structure may be formed from polysilicon while the bottom electrode may be formed from titanium nitride ("TiN"). Alternatively, one sacrificial structure may be formed from TiN while a second sacrificial structure may be formed from polysilicon. Conventional etching conditions, such as a wet etch process or a dry etch process, may be used to remove the sacrificial structure. In addition, one sacrificial structure may be removed without removing other sacrificial structures on the semiconductor wafer. For instance, a sacrificial plug may be removed from the opening without removing a sacrificial liner. The sacrificial liner may subsequently be removed from the opening without removing or damaging other components on the semiconductor wafer, such as the bottom electrode. When the sacrificial structure is removed, space previously occupied by the sacrificial structure may be used to form the ~~double-sided~~ double-sided capacitor or the contact.

Please amend paragraph number **[0026]** as follows:

**[0026]** The sacrificial structure, such as the sacrificial liner or the sacrificial plug, may be deposited in the opening 70 and used to maintain space in the opening 70 that will ultimately be used in forming the double-sided capacitor or the contact. The sacrificial structure may be

selectively removed from the opening 70, providing additional space in which to form the ~~double-sided~~ double-sided capacitor or the contact. In other words, the space previously occupied by the sacrificial structure may ultimately be occupied by the top electrode and dielectric layer of the double-sided capacitor or by a conductive layer of the contact. As described in detail herein, this may provide usable surface area from both the ~~frontside~~ front side and ~~backside~~ back side of the bottom electrode.

Please amend paragraph number **[0036]** as follows:

**[0036]** A third insulating layer 150 may be formed over the second insulating layer 62, as shown in FIG. 16. The third insulating layer 150 may be formed from BPSG or PSG. An opening 70′ may be formed in the third insulating layer 150 and extended through to the top surface of the second insulating layer 62 so that the opening 70′ is substantially aligned with opening 70. Sacrificial liner 90′ may be deposited in the opening 70′ so that it covers the sidewalls of opening 70′ and over a top surface of the third insulating layer 150 (see FIG. 17). The sacrificial liner 90 and sacrificial liner 90′ may be substantially aligned. As shown in FIG. 17, portions of the sacrificial liner 90′ extending over the top surface of the third insulating layer 150 may be removed, such as by CMP or by etching so that the sacrificial liner 90′ lines the sidewalls of the opening 70′. Alternatively, the sacrificial liner 90 may be removed from opening 70, such as by using an etch solution of 5%-15% $H_2O_2$, 60%-90% $H_2SO_4$, and 5%-15% $H_2O$ at a temperature of approximately 90°C to approximately 150°C. It is also contemplated that additional etch solutions that selectively remove the sacrificial liner 90 without damaging or removing other structures on the semiconductor wafer may be used. A single sacrificial liner 90″ may then be deposited in openings 70 and 70′, as shown in FIG. 18.

Please amend paragraph number **[0043]** as follows:

**[0043]** It is also contemplated that portions of the double-sided capacitor 134 may be formed in openings 70, 70′ at the same time as portions of the contact 250 are formed in openings 70″, 70‴ as shown in FIGs. 28 and 29. As shown in FIG. 28, openings 70 and 70″ for the ~~double-~~

~~sided~~ double-sided capacitor 134 and the contact plug 250, respectively, may be simultaneously formed in the second insulating layer 62. The openings 70, 70″ may be formed as previously described. Openings 70, 70″ may be sequentially formed in the second insulating layer 62 without departing from the scope of the present invention. The sacrificial liner 90 and the sacrificial plug 142 may be formed in each of the openings 70, 70″, as shown in FIG. 29. The sacrificial liner 90 and the sacrificial plug 142 may be formed as described above.